# MT3004

## N-Channel Enhancement Mode Field Effect Transistor

MT Semiconductor®

http://www.mtsemi.com

### Product Summary

- $V_{DS}$ = 30V
- $I_D$ = 80A
- $R_{DS(ON)}$ = 3.5mΩ@$V_{GS}$=10V
- $R_{DS(ON)}$ = 5.0 mΩ@$V_{GS}$=4.5V

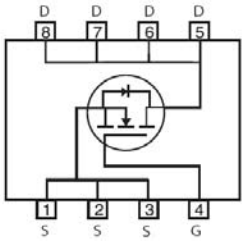
### Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

### Applications

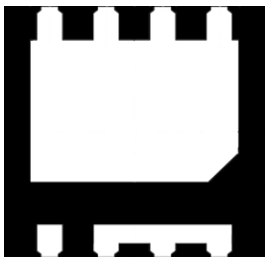
- Notebook Computer
- Portable Battery Pack

### Simplified Schematic




### MARKING DIAGRAM & PIN ASSIGNMENT

DFN3X3-8L



PIN1

| Absolute Maximum Ratings $T_A$=25℃ unless otherwise noted | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Maximum** | **Units** |
| Drain-Source Voltage | | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current [AF] | $T_A$=25℃ | $I_{DSM}$ | 80 | A |
| | $T_A$=70℃ | | 65 | |
| Pulsed Drain Current [B] | | $I_{DM}$ | 160 | A |
| Avalanche Current [C] | | $I_{AR}$ | 42 | A |
| Repetitive avalanche energy L=0.3mH [C] | | $E_{AR}$ | 75 | mJ |
| Power Dissipation | $T_A$=25℃ | $P_{DSM}$ | 2.8 | W |
| | $T_A$=70℃ | | 1.6 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | ℃ |

| Thermal Characteristics | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typ** | **Max** | **Units** |
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 32 | 40 | ℃/W |
| Maximum Junction-to-Ambient [A] | Steady-State | | 60 | 75 | ℃/W |
| Maximum Junction-to-Lead [C] | Steady-State | $R_{\theta JL}$ | 16 | 24 | ℃/W |

**Electrical Characteristics ($T_J$=25℃ unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250uA, $V_{GS}$=0V | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=24V, $V_{GS}$=0V | | | 1 | uA |
| | | $T_J$=85℃ | | | 100 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±20V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250μA | 0.8 | 1.5 | 2.0 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 100 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=15A | | 3.5 | 4.5 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=15A | | 5.0 | 7.8 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=20A | | 68 | | S |
| $V_{SD}$ | Diode Forward Voltage | $V_{GS}$=0V, $I_S$=40A | | 0.7 | 1.3 | V |
| $I_S$ | Maximum Body-Diode + Schottky Continuous Current | | | | 50 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=15V, f=1MHz | | 1920 | 2260 | pF |
| $C_{oss}$ | Output Capacitance | | | 750 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 68 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 0.8 | 1.2 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=20A | | 29 | 35 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 14 | 16 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 4.6 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 4.6 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=15V, $R_L$=1.2Ω, $R_{GEN}$=3Ω | | 5.5 | | ns |
| $t_r$ | Turn-On Rise Time | | | 5.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 25 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 4.3 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=20A, dI/dt=500A/ μs | | 15 | 17 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=20A, dI/dt=500A/ μs | | 32 | 38 | nC |

A: The value of $R_{\theta JA}$ is measured withthe device mounted on 1in $^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25℃. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25℃. The SOA curve provides a single pulse rating.

F. The current rating is based on the t ≤ 10s thermal resistance rating.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

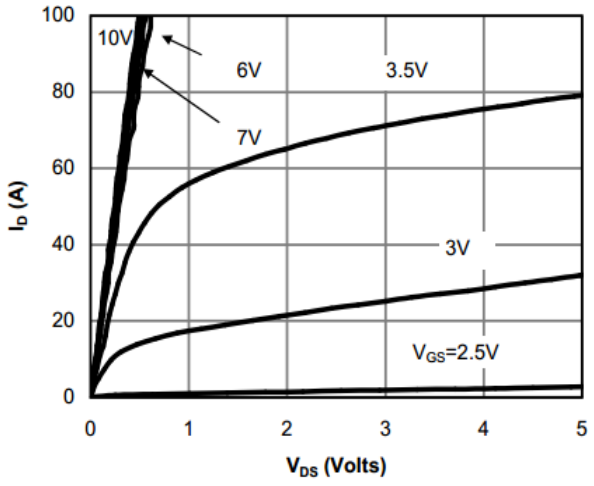



Fig 1: On-Region Characteristics (Note E)

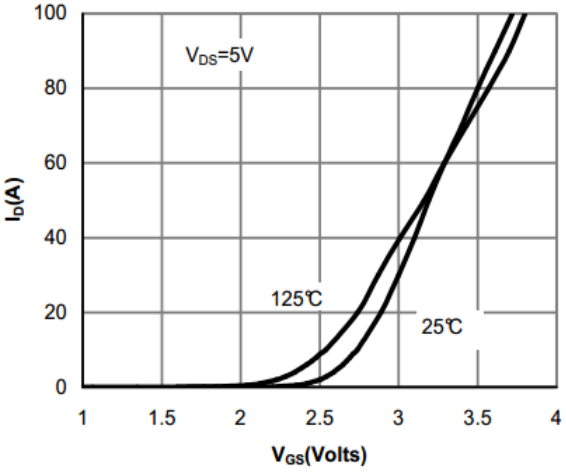



Figure 2: Transfer Characteristics (Note E)

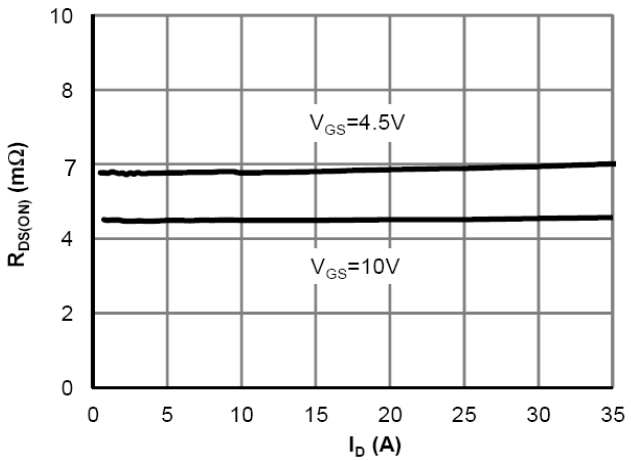



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

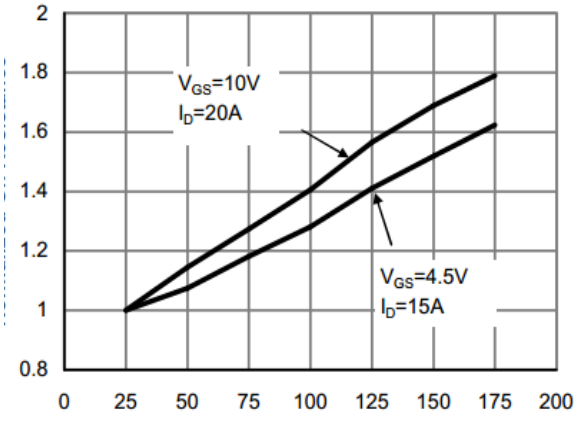



Figure 4: On-Resistance vs. Junction Temperature (Note E)

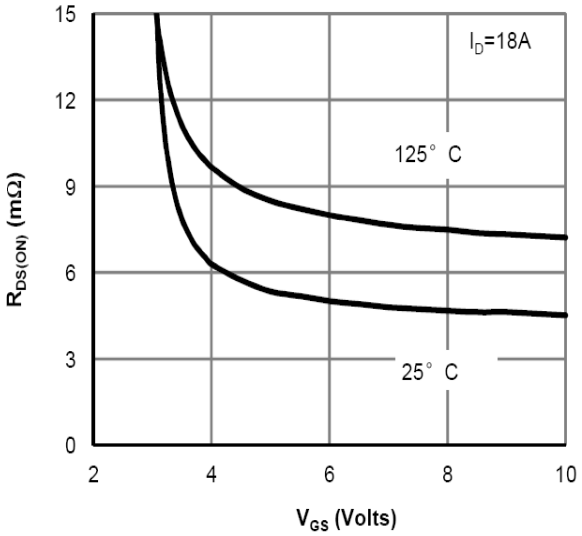



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

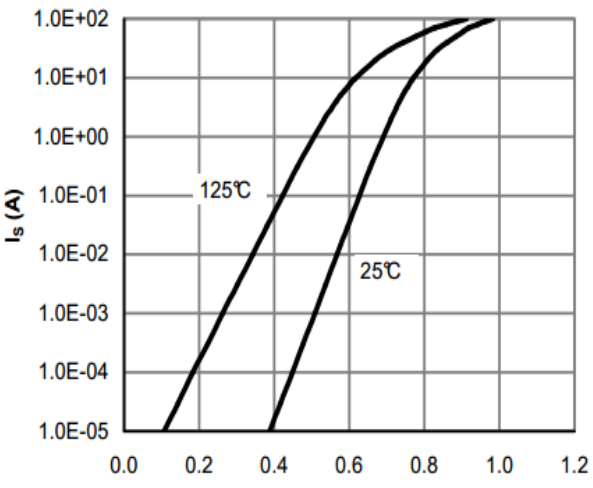



Figure 6: Body-Diode Characteristics (Note E)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

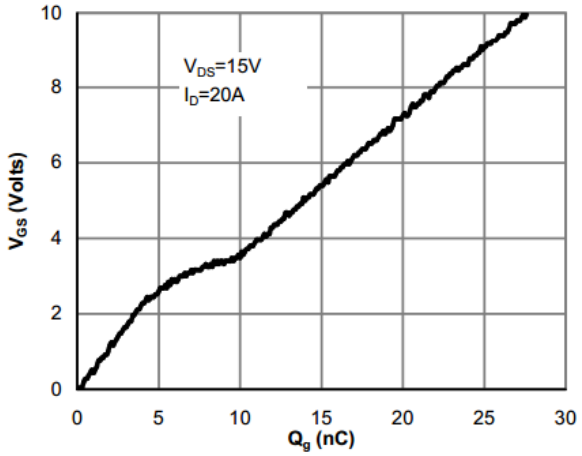



Figure 7: Gate-Charge Characteristics

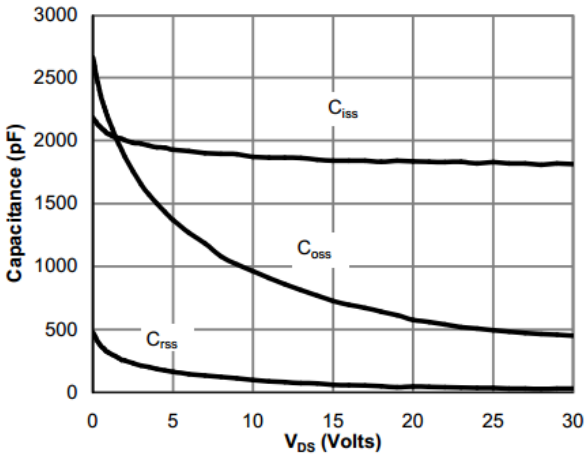



Figure 8: Capacitance Characteristics

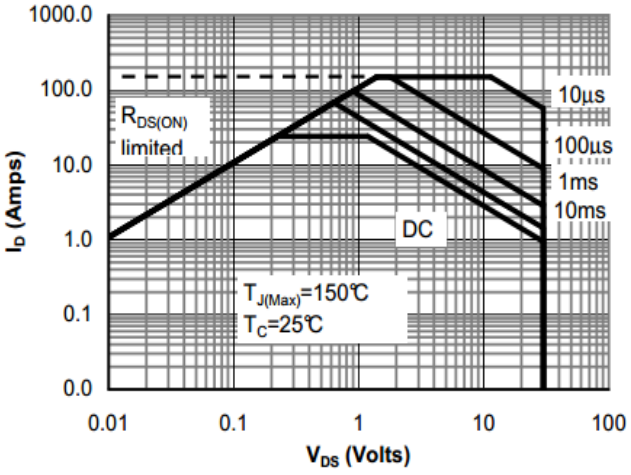



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

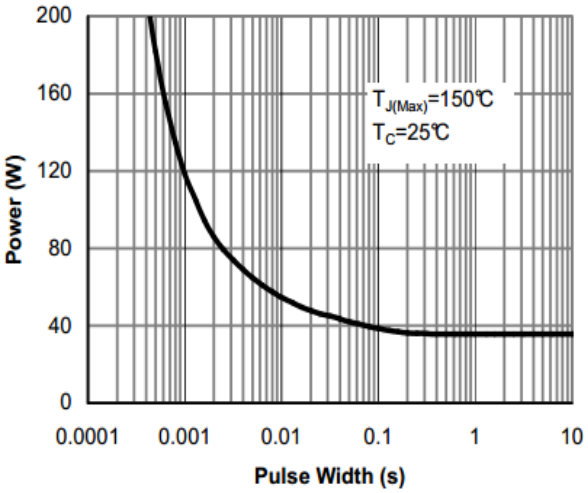



Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

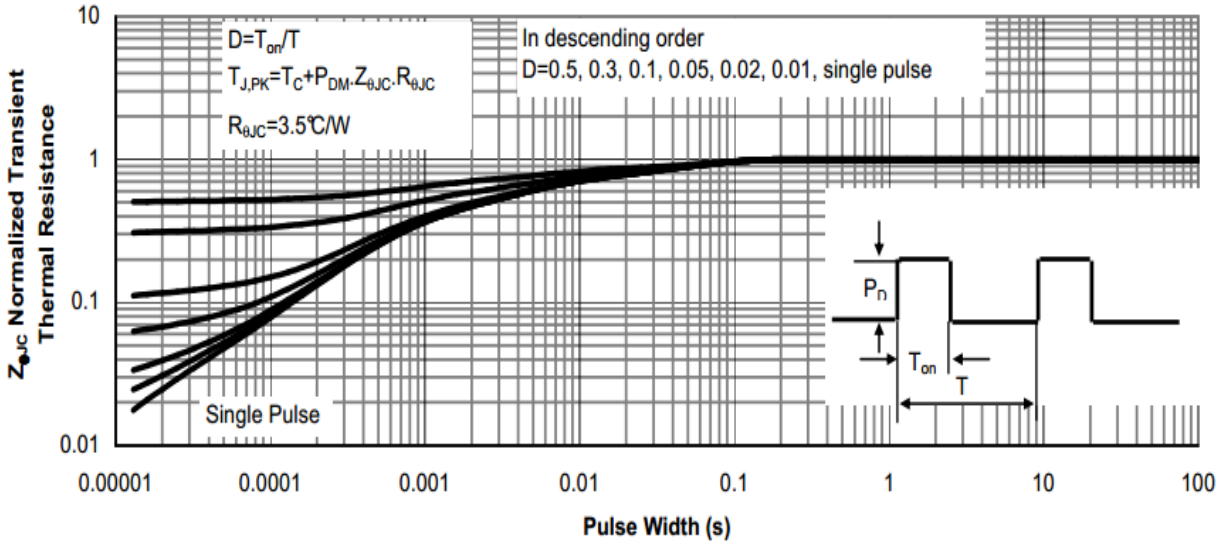
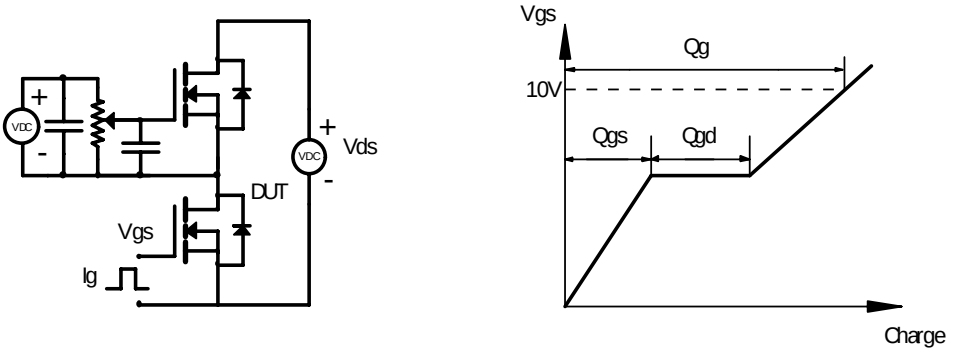
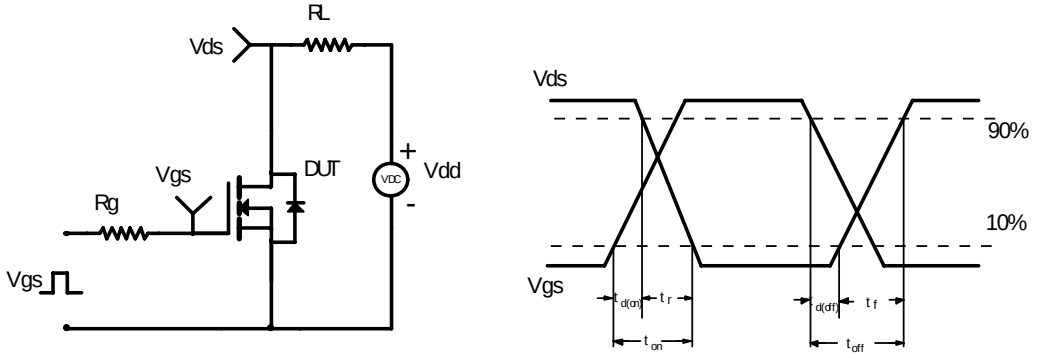



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

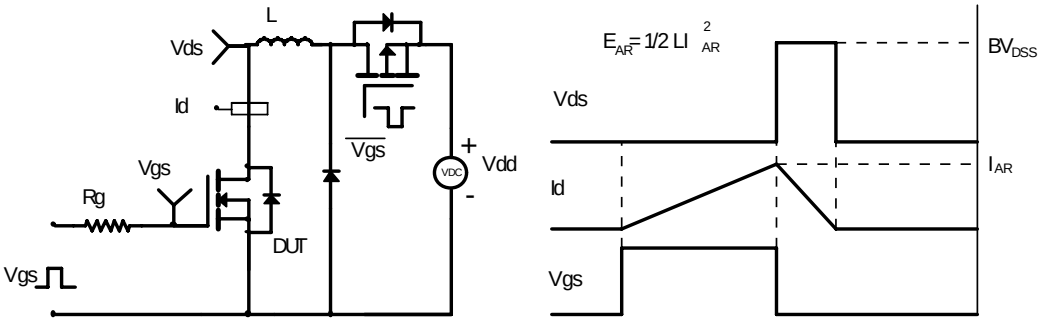
Gate Charge Test Circuit & Waveform



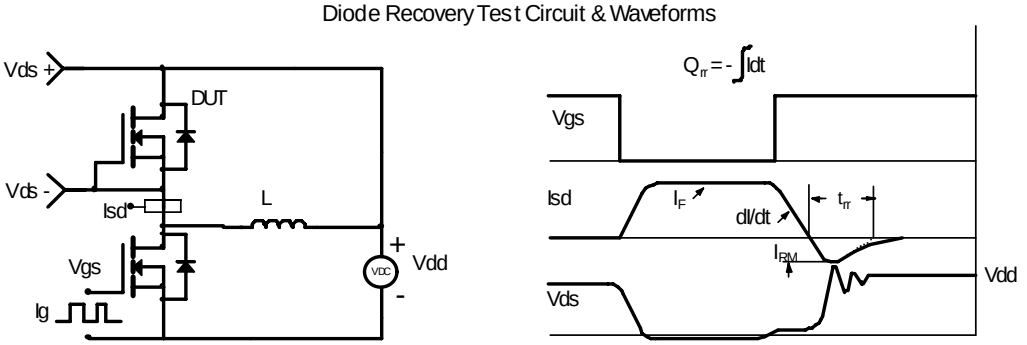

Resistive Switching Test Circuit & Waveforms



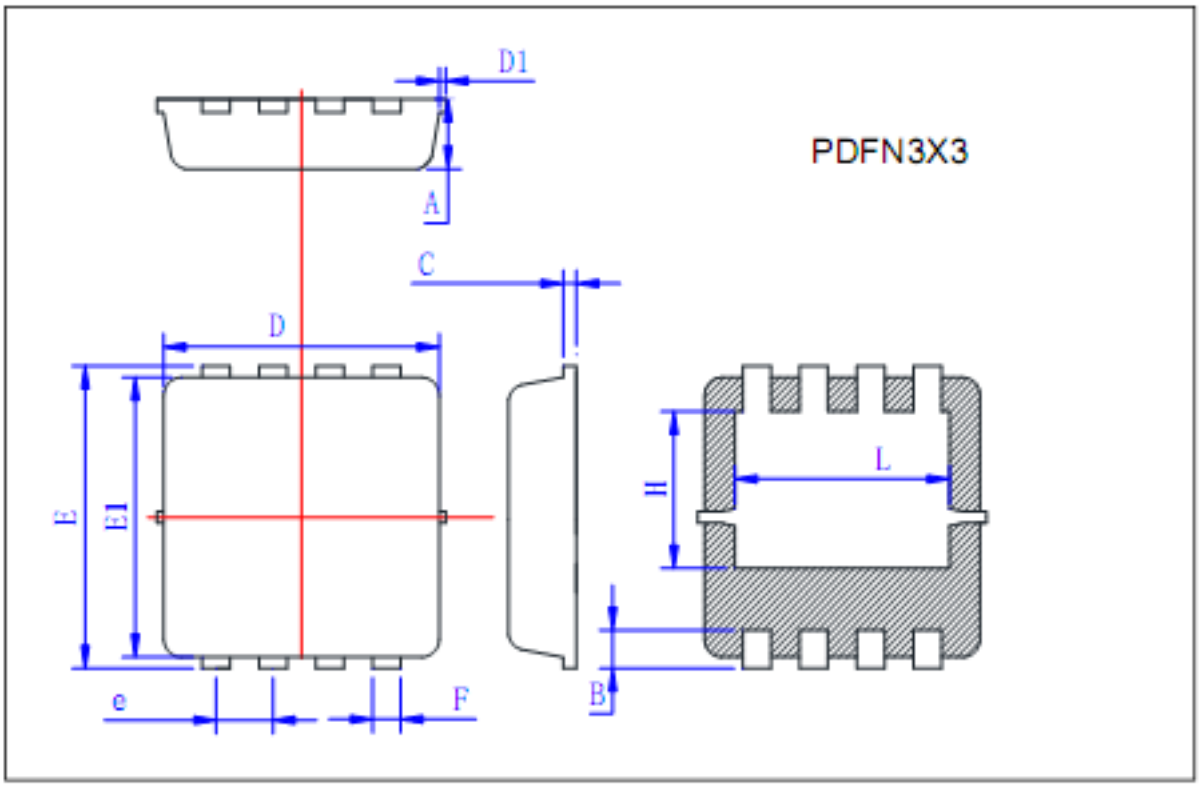

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




Diode Recovery Test Circuit & Waveforms



# PACKAGE OUTLINE DIMENSIONS




| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 0.725 | 0.775 | 0.825 |
| B | 0.28 | 0.38 | 0.48 |
| C | 0.13 | 0.15 | 0.20 |
| D | 3.05 | 3.15 | 3.25 |
| D1 | | | 0.10 |
| E | 3.25 | 3.35 | 3.45 |
| E1 | 3.0 | 3.1 | 3.2 |
| e | 0.60 | 0.65 | 0.70 |
| F | 0.27 | 0.32 | 0.37 |
| H | 1.63 | 1.73 | 1.83 |
| L | 2.35 | 2.45 | 2.55 |

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