# MT4015N5

## N-Channel Enhancement Mode Field Effect Transistor

MT Semiconductor®

http://www.mtsemi.com

### Product Summary

- $V_{DS}$ = 40V
- $I_D$ = 160A ($V_{GS}$ = 10V)
- $R_{DS(ON)}$= 1.7 mΩ @$V_{GS}$ =10V
- $R_{DS(ON)}$ = 2.2 mΩ @$V_{GS}$ =4.5V

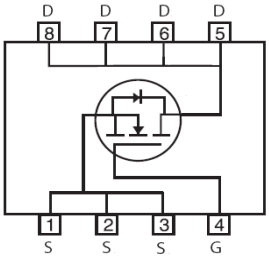
### Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.
- PDFN5x6-8L Package

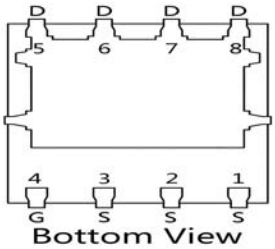
### Applications

- Portable Equipment and Battery Powered Systems.
- Power Management in Notebook Computers.

### Simplified Schematic




### MARKING DIAGRAM & PIN ASSIGNMENT




## Absolute Maximum Ratings ($T_A$ = 25℃ unless otherwise noted)

| Symbol | Parameter | | Steady State | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | | 40 | V |
| $V_{GS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Continuous Drain Current [1] | $T_C$ = 25℃ | 160 | A |
| $I_{DM}$ | Pulsed Drain Current [2] | | 300 | A |
| $I_S$ | Continuous Source Current (Diode Conduction) [1] | | 60 | A |
| $E_{AS}$ | Single Pulse Drain-Source Avalanche Energy [3] | | 110 | mJ |
| $P_D$ | Maximum Power Dissipation | $T_A$ = 25℃ | 2 | W |
| | | $T_C$ = 25℃ | 89 | |
| $T_J$, $T_{STG}$ | Operating Junction and Storage Temperature Range | | -55~150 | ℃ |

Notes:

1. Surface Mounted on 1” x 1” FR4 Board, t≦10 Sec.
2. Pulse width limited by maximum junction temperature.
3. The test condition is $T_J$ =25℃, $V_{DD}$=30V, $V_{GS}$=10V, L=0.1mH, $R_G$=25Ω, $I_{AS}$=50A.

## Thermal Resistance Ratings

| Symbol | Parameter | Typical | Maximum | Unit |
|---|---|---|---|---|
| $R_{thJA}$ | Maximum Junction-to-Ambient | - | 62.5 | ℃/W |
| $R_{thJC}$ | Maximum Junction-to-Case | - | 1.4 | |

## Electrical Characteristics ($T_A$=25°C, unless otherwise noted)

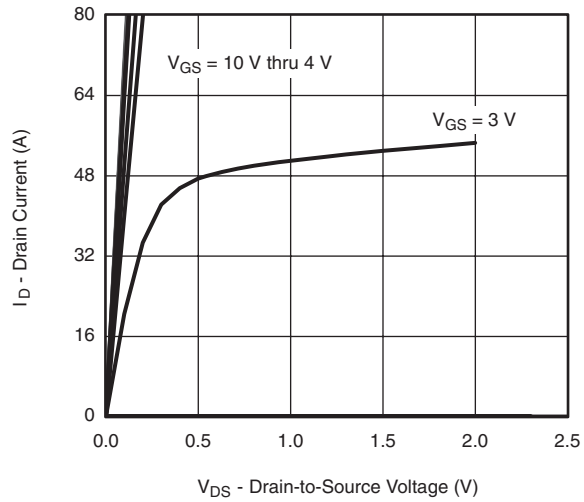
| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$= 0V, $I_D$= 250μA | 40 | - | - | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA | 1.0 | - | 2.2 | V |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | - | - | ±100 | nA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 40V, $V_{GS}$ = 0V | - | | 1 | μA |
| | | $V_{DS}$ = 40V, $V_{GS}$ = 0V, $T_J$ = 85℃ | - | | 30 | |
| $R_{DS(on)}$ | Drain Source On State Resistance [a] | $V_{GS}$ = 10V, $I_D$ = 30A | - | 1.7 | 2.2 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 20A | - | 2.2 | 3.8 | |
| $V_{SD}$ | Diode Forward Voltage [a] | $V_{GS}$ = 0V, $I_S$ = 40A | - | 0.82 | 1.3 | V |
| **Dynamic Characteristics** [b] | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$= 15V, $V_{GS}$= 0V, f = 1MHz | - | 3520 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 1210 | - | |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 390 | - | |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 15V, $V_{GS}$ = 10V, $I_D$ = 20A | - | 41 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 15 | - | |
| $Q_{gd}$ | Gate-Drain Charge | | - | 12 | - | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 15V, $V_{GS}$ = 4.5V<br>$I_D$ = 20A, $R_{GEN}$ = 3Ω | - | 22 | - | nSec |
| $t_r$ | Rise Time | | - | 35 | - | |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 50 | - | |
| $t_f$ | Fall Time | | - | 27 | - | |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$ =20A, di/dt= 100A/μA, $T_J$=25℃ | - | 33 | - | nSec |

Note:

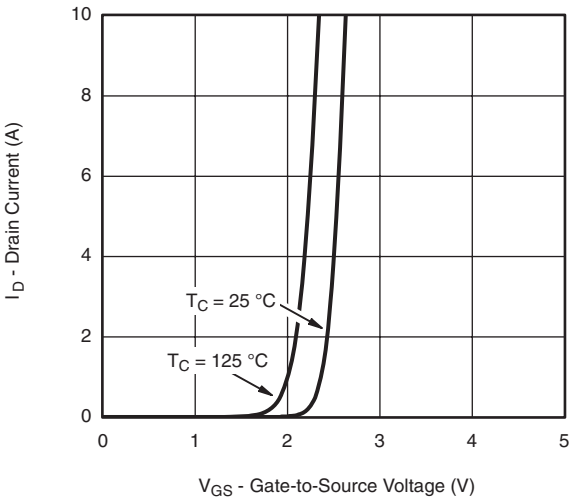
a. Pulse test; pulse width≦300μs, duty cycle≦2%.

b. Guaranteed by design, not subject to production testing.

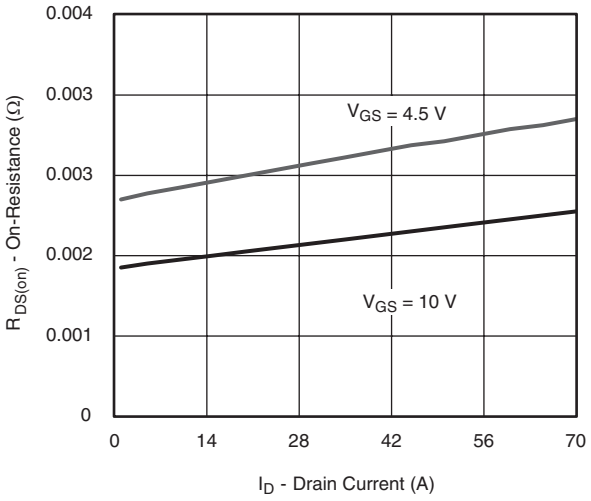
# Characteristics Curve



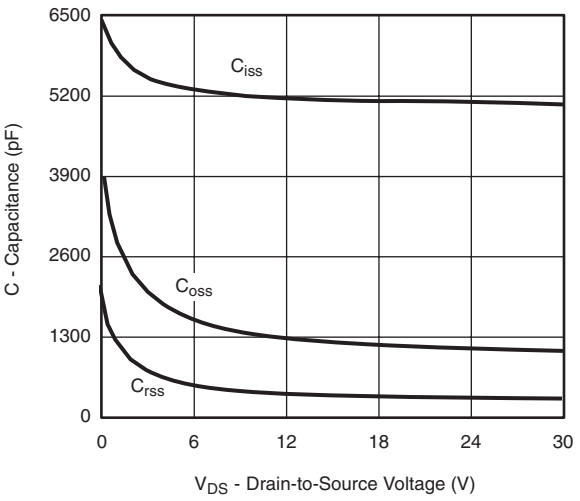

**Output Characteristics**



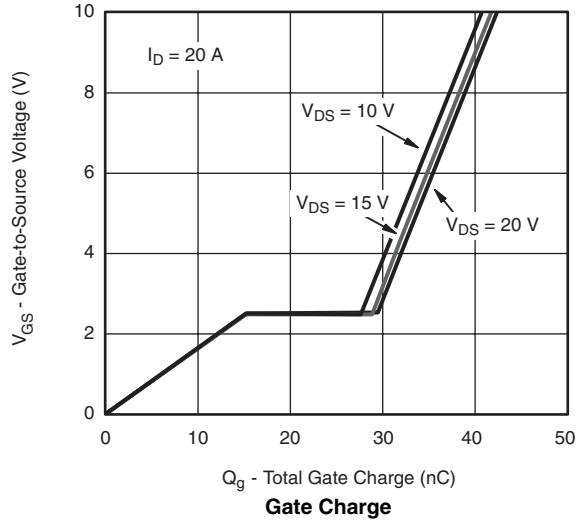

**Transfer Characteristics**



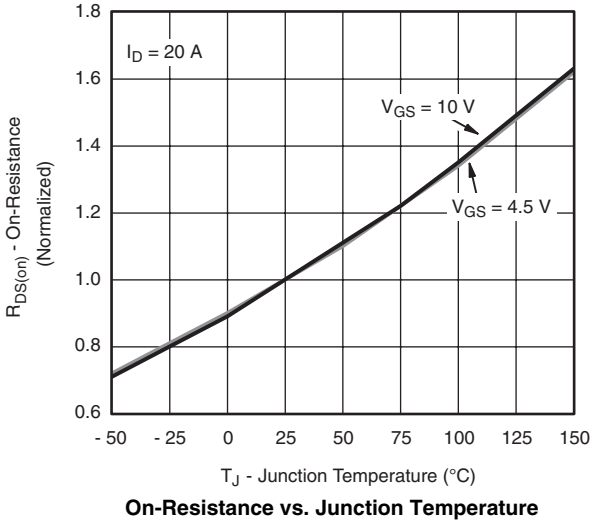

**On-Resistance vs. Drain Current**




**Capacitance**

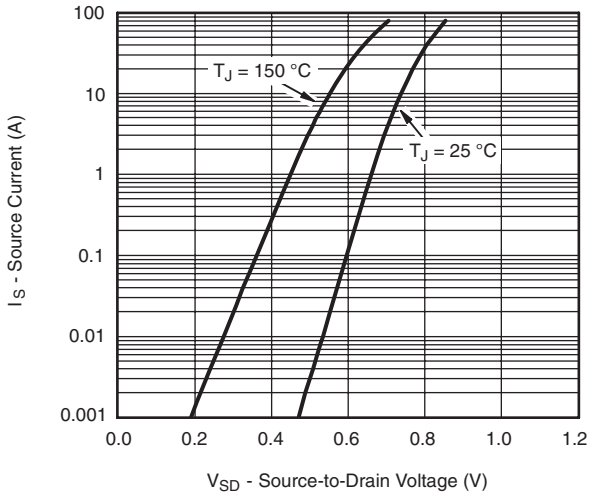



**Gate Charge**

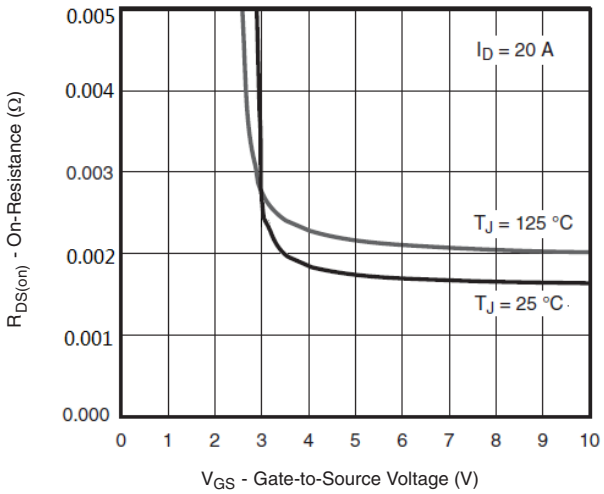



**On-Resistance vs. Junction Temperature**

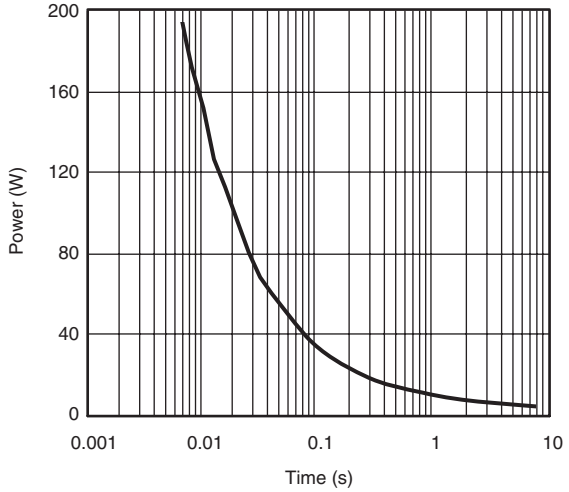
# Characteristics Curve



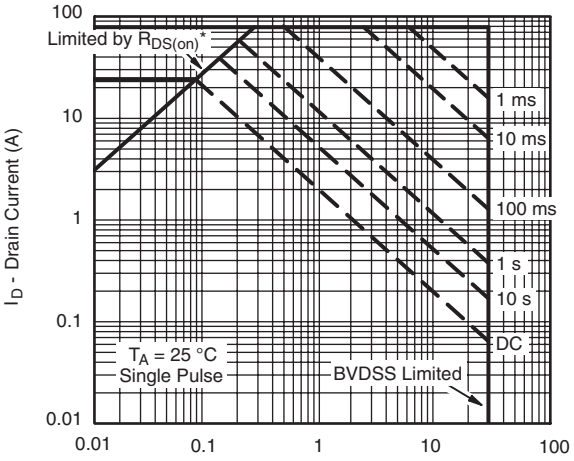

**Source-Drain Diode Forward Voltage**




**On-Resistance vs. Gate-to-Source Voltage**

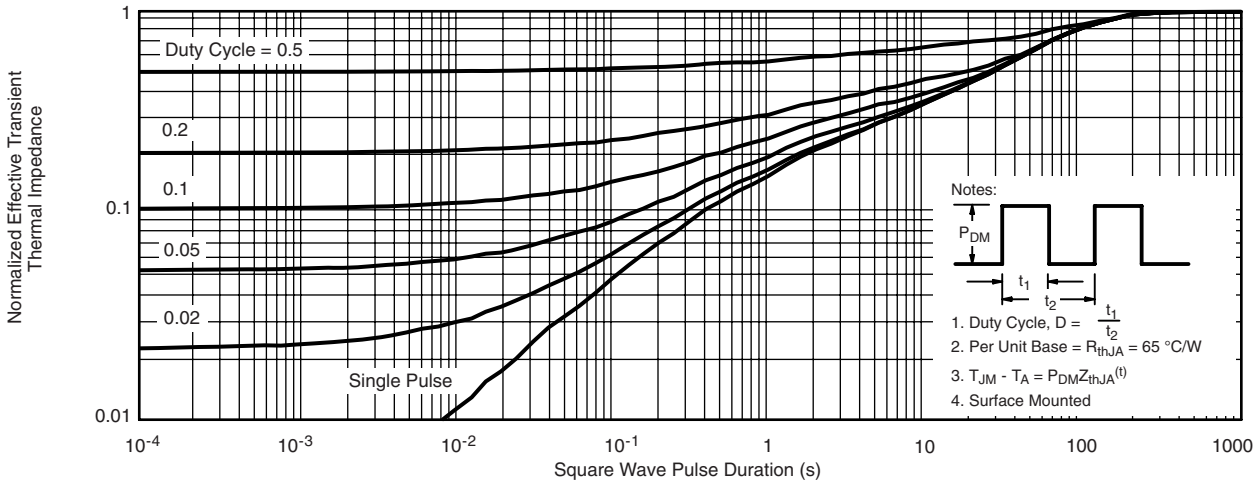



**Single Pulse Power, Junction-to-Ambient**



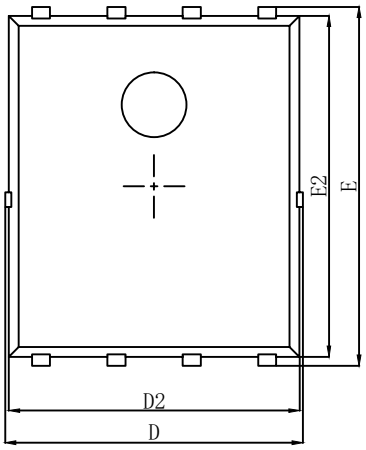

* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Safe Operating Area, Junction-to-Ambient**

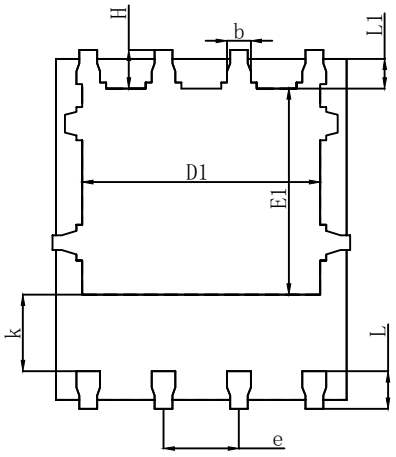



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

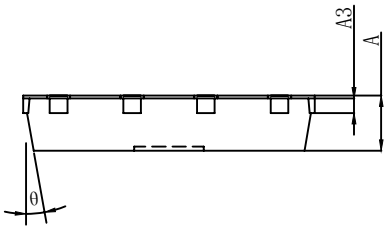
PDFNWB5×6-8L(P1.27T0.95) PACKAGE OUTLINE DIMENSIONS




Top View
[顶视图]




Bottom View
[背视图]




Side View
[侧视图]

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.900 | 1.000 | 0.035 | 0.039 |
| A3 | 0.254REF. | | 0.010REF. | |
| D | 4.944 | 5.096 | 0.195 | 0.201 |
| E | 5.974 | 6.126 | 0.235 | 0.241 |
| D1 | 3.910 | 4.110 | 0.154 | 0.162 |
| E1 | 3.375 | 3.575 | 0.133 | 0.141 |
| D2 | 4.824 | 4.976 | 0.190 | 0.196 |
| E2 | 5.674 | 5.826 | 0.223 | 0.229 |
| k | 1.190 | 1.390 | 0.047 | 0.055 |
| b | 0.350 | 0.450 | 0.014 | 0.018 |
| e | 1.270TYP. | | 0.050TYP. | |
| L | 0.559 | 0.711 | 0.022 | 0.028 |
| L1 | 0.424 | 0.576 | 0.017 | 0.023 |
| H | 0.574 | 0.726 | 0.023 | 0.029 |
| θ | 10° | 12° | 10° | 12° |

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