MT4407

P-Channel MOSFET
-30V, -12A, 13mΩ

MT Semiconductor®

http://www.mtsemi.com

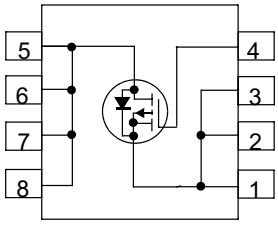
General Description

This P-channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.
This device is well suited for Power Management and Load switching applications common in Notebook computers and Portable Battery Packs.

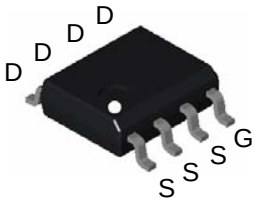
Features

- $R_{DS(on)}$ = 13mΩ @ V_{GS} = -10V, I_D = -12A
- $R_{DS(on)}$ = 20mΩ @ V_{GS} = -4.5V, I_D = -12A
- Extended V_{GS} range (-25V) for battery applications
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- RoHS compliant

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



SO-8

Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		-30	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current -Continuous	(Note1a)	-12	A
	-Pulsed		-75	A
P_D	Power Dissipation for Single Operation	(Note1a)	2.5	W
		(Note1b)	1.2	
		(Note1c)	1.0	
T_J, T_{STG}	Operating and Storage Temperature		-55 to 150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance , Junction to Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance , Junction to Case (Note 1)	25	°C/W

Package Marking and Ordering Information

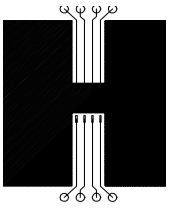
Device Marking	Device	Reel Size	Tape Width	Quantity
MT4407	MT4407	13"	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

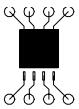
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-30			V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		-20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24V, V_{GS} = 0V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25V, V_{DS} = 0V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-1	-1.9	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		8.1		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = -10V , I_D = -12A		13	15	mΩ
		V_{GS} = -4.5V, I_D = -12A		20	22	
		V_{GS} = -10V, I_D = -12A T_J = 125°C		17	22	
g_{FS}	Forward Transconductance	V_{DS} = -5V, I_D = -12A		60		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz		1200		pF
C_{oss}	Output Capacitance			400		pF
C_{rss}	Reverse Transfer Capacitance			160	190	pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15V, I_D = -1A V_{GS} = -10V, R_{GS} = 6Ω		7		ns
t_r	Rise Time			9	12	ns
$t_{d(off)}$	Turn-Off Delay Time			25.6	28	ns
t_f	Fall Time			12	16	ns
Q_g	Total Gate Charge	V_{DS} = -15V, V_{GS} = -10V, I_D = -12A		88	124	nC
Q_g	Total Gate Charge	V_{DS} = -15V, V_{GS} = -5V, I_D = -12A		46	65	nC
Q_{gs}	Gate to Source Gate Charge			8		nC
Q_{gd}	Gate to Drain Charge			23.5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -2.1A		-0.7	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = 12A, di/dt = 100A/μs			45	ns
Q_{rr}	Reverse Recovery Charge	I_F = 12A, di/dt = 100A/μs			34	nC

Notes:

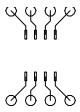
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W (10 sec) when mounted on a 1 in^2 pad of 2 oz copper



b) 105 °C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125 °C/W when mounted on a minimun pad

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

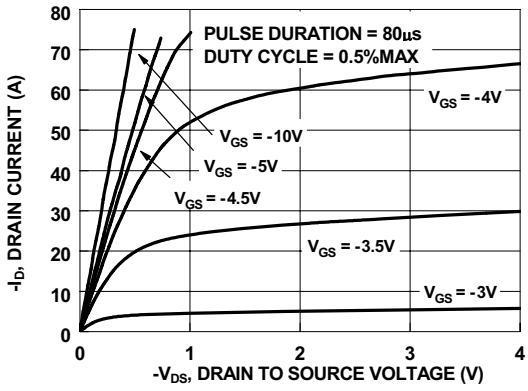


Figure 1. On Region Characteristics

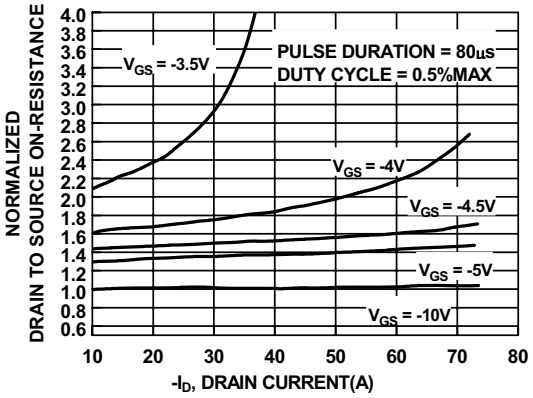


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

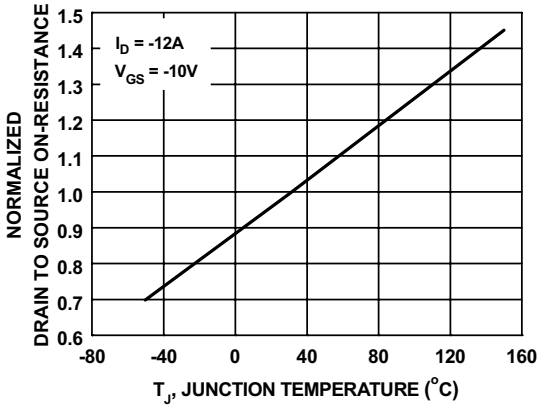


Figure 3. Normalized On Resistance vs Junction Temperature

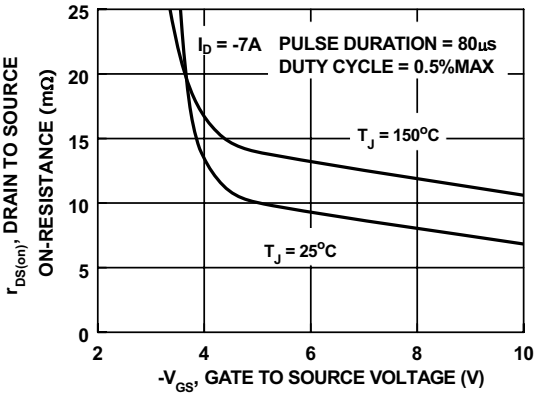


Figure 4. On-Resistance vs Gate to Source Voltage

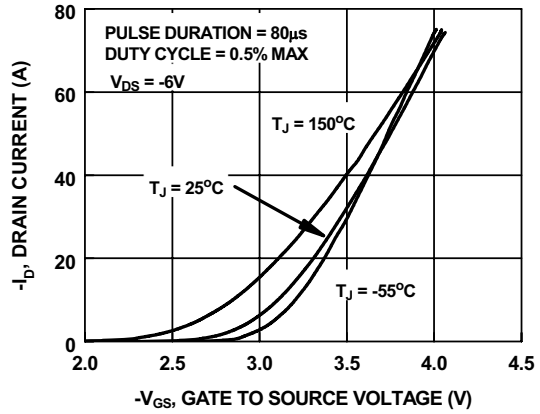


Figure 5. Transfer Characteristics

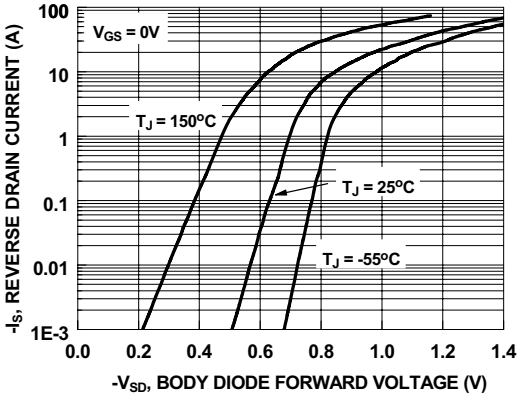


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

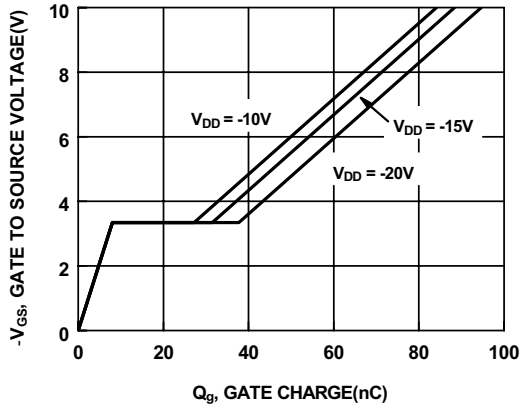


Figure 7. Gate Charge Characteristics

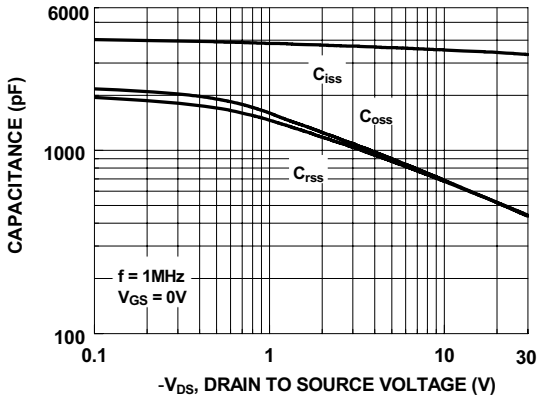


Figure 8. Capacitance vs Drain to Source Voltage

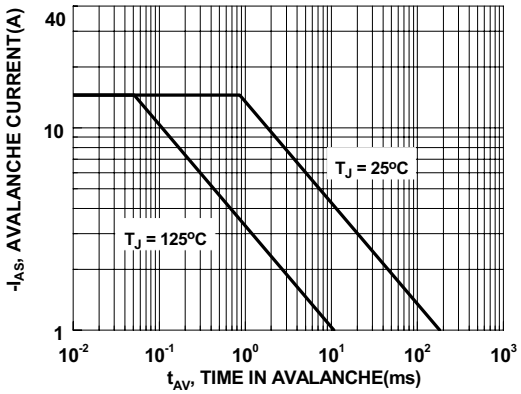


Figure 9. Unclamped Inductive Switching Capability

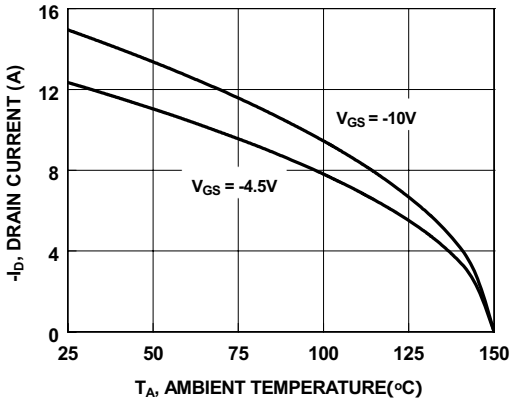


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

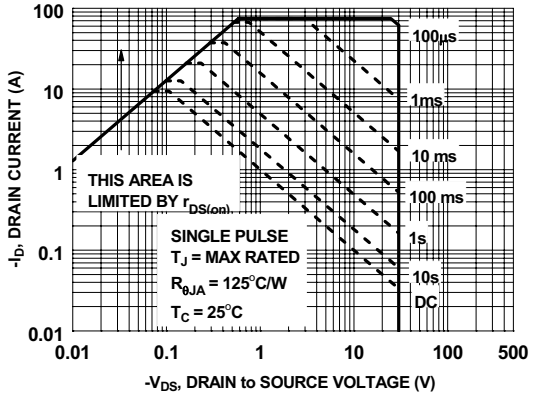


Figure 11. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25 °C unless otherwise noted

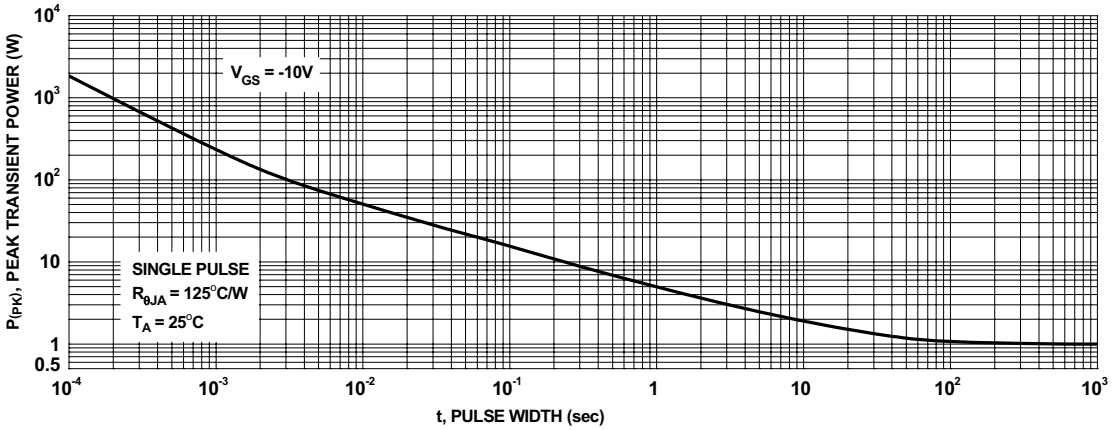


Figure 13. Single Pulse Maximum Power Dissipation

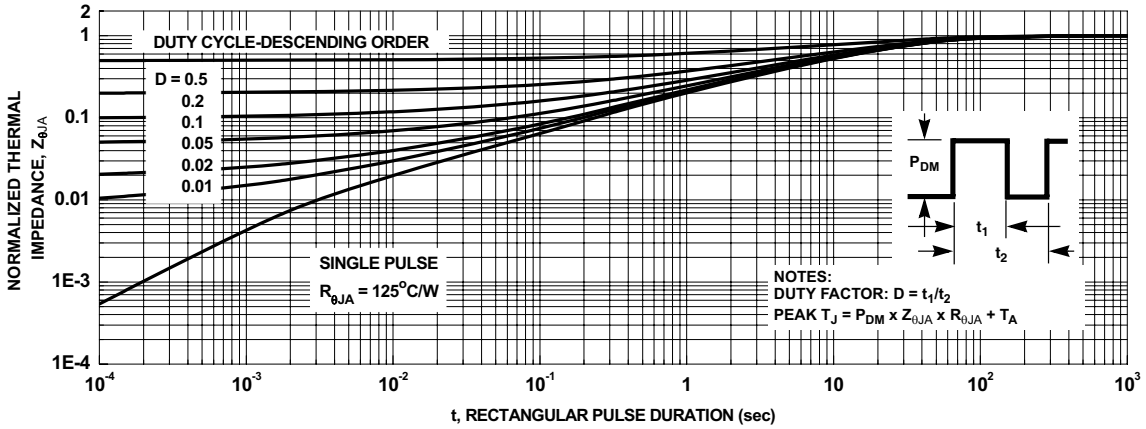
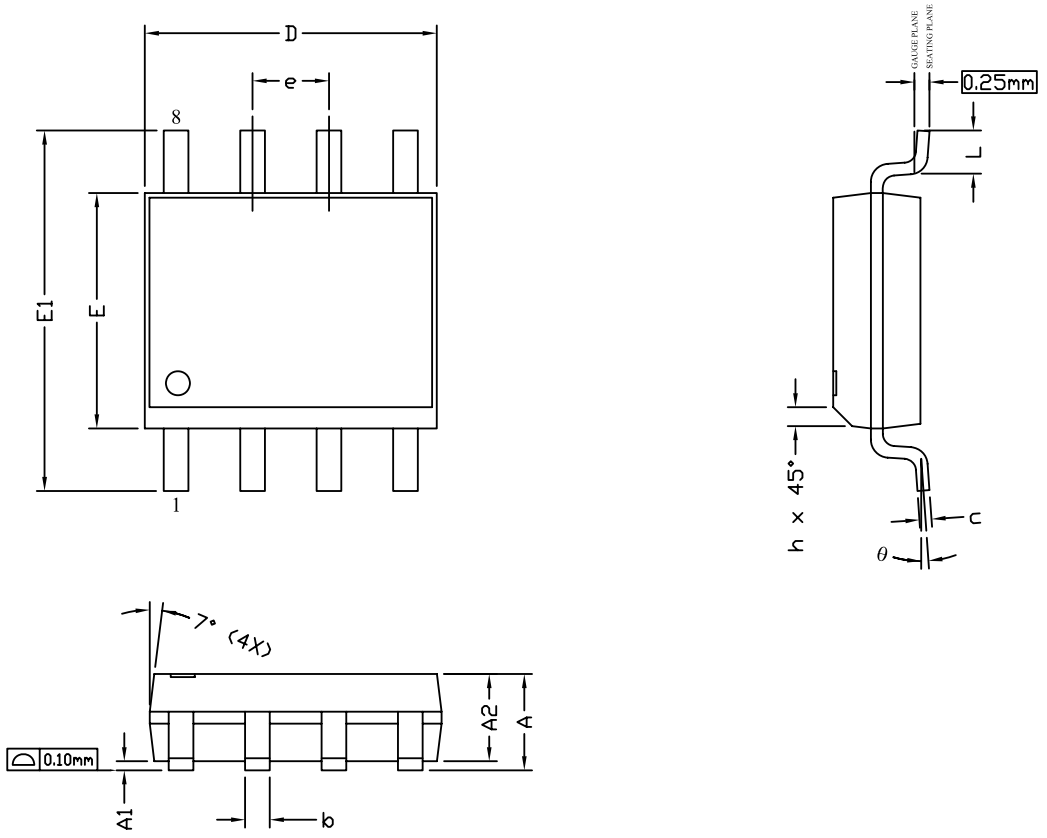


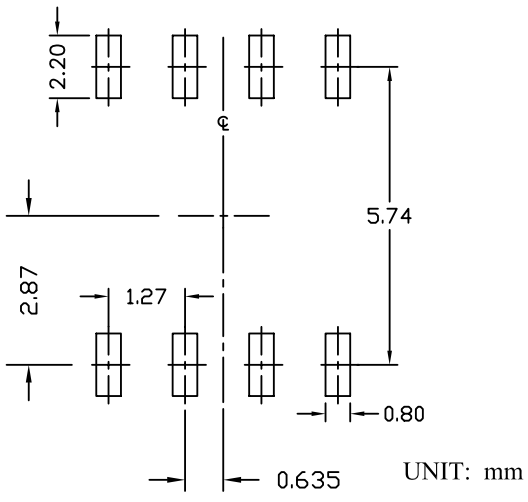
Figure 14. Junction-to-Ambient Transient Thermal Response Curve

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SO8 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN

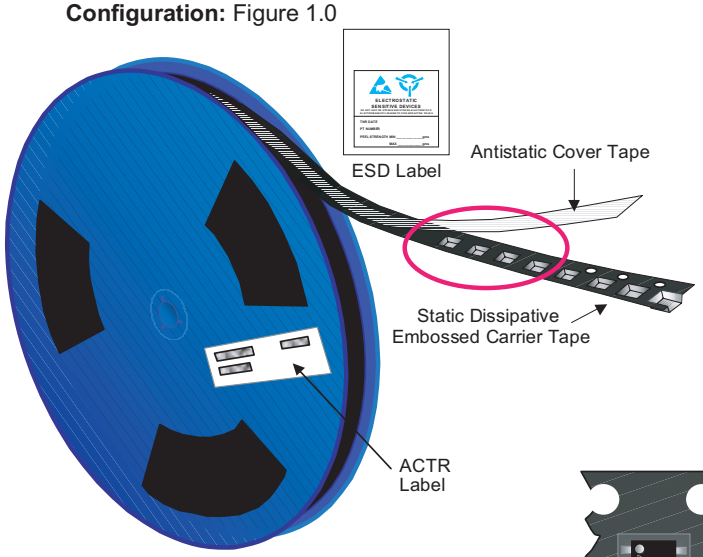


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	----	0.25	0.004	----	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	----	0.51	0.012	----	0.020
c	0.17	----	0.25	0.007	----	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	----	0.50	0.010	----	0.020
L	0.40	----	1.27	0.016	----	0.050
θ	0°	----	8°	0°	----	8°

NOTE
1. ALL DIMENSIONS ARE IN MILLMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SOIC-8 Tape and Reel Data

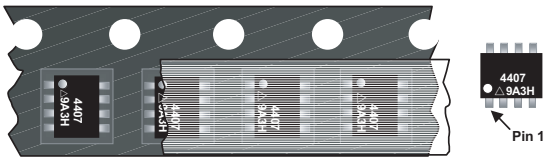
SOIC(8lds) Packaging
Configuration: Figure 1.0



Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

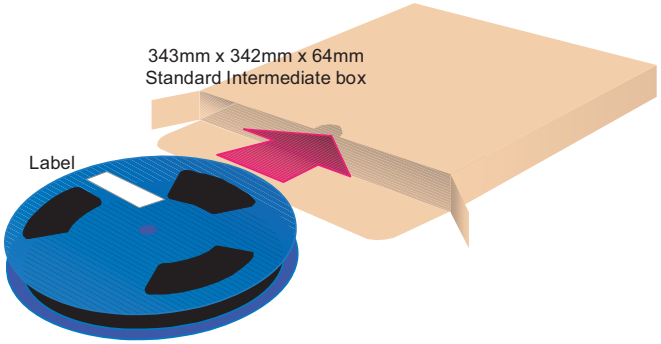


SOIC-8 Unit Orientation

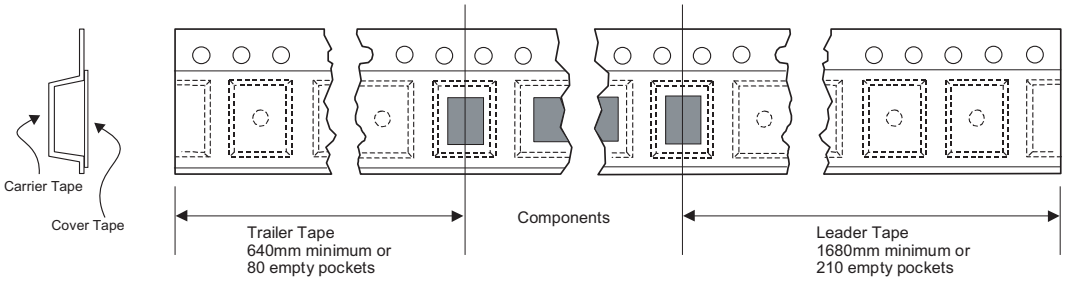
SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	ACTR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

MT4407ACTR Label sample

XH1 MT4407ACTR 2500 QTY: 2500
XH2 C97H22K2-9A3H-K143 P6070561 SPEC:
-MOS-TECH SEMICONDUCTOR LTD-



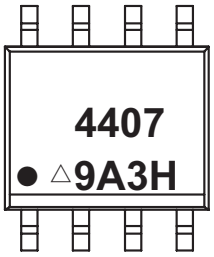
SOIC(8lds) Tape Leader and Trailer
Configuration: Figure 2.0



Part Marking Information

SO-8 (PMG Code)

SO-8 Devices



4407 = Example Base Part Number
● = Pin 1 Indicator
△ = ESD Symbol
9 = Year Code
A = Month Code
3 = Week Code
H = Assembly Factory Code

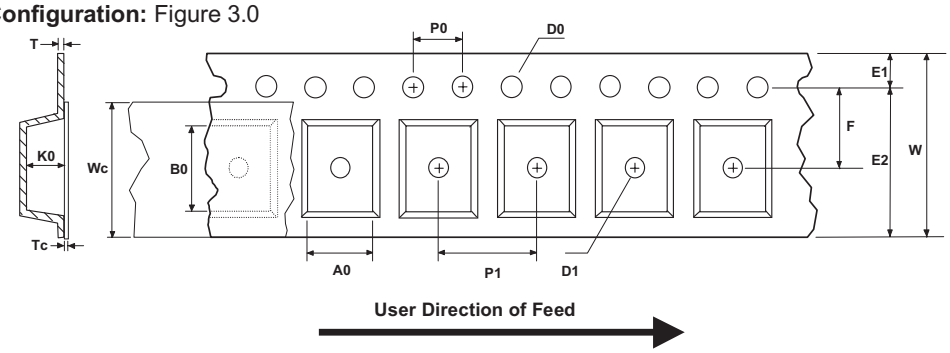
NOTE:

1. For analog switches base part includes DG prefix. Package suffix may or may not be present, depending on room available.

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

SOIC-8 Tape and Reel Data, continued

SOIC(8lds) Embossed Carrier Tape
Configuration: Figure 3.0

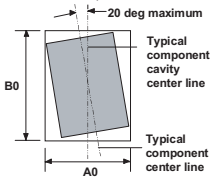


Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

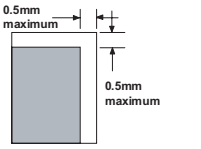
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

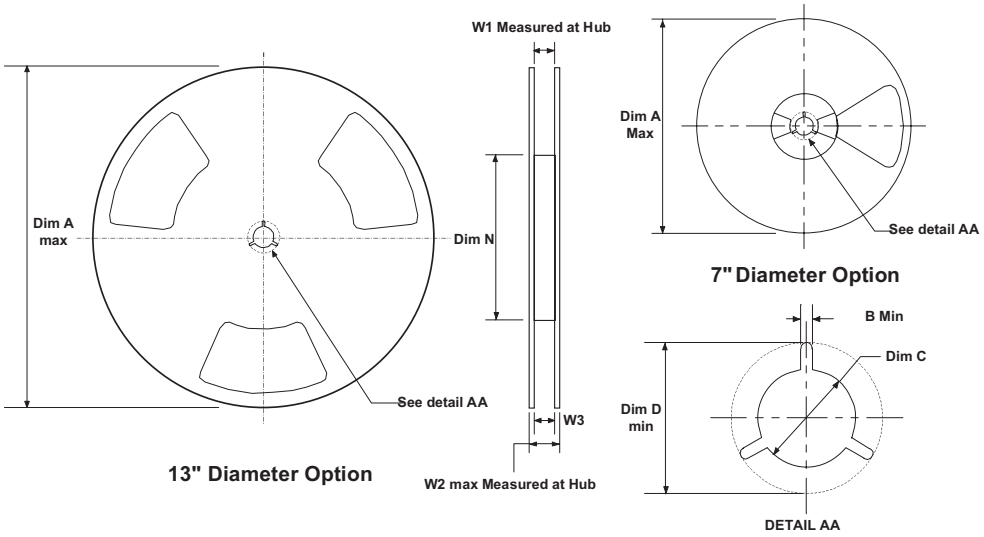


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4

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