# MT8102

## P-Channel MOSFET
## -30V, -15A, 6.0mΩ

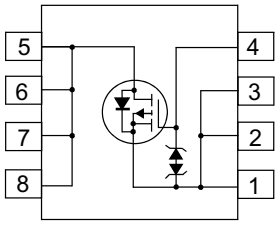
MT Semiconductor®

http://www.mtsemi.com

## General Description

This N-channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance This device is well suited for Power Management and Load switching applications common in Notebook computers and Portable Battery Packs.

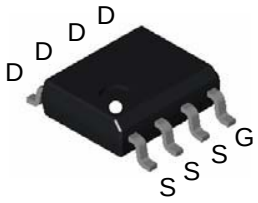
## Simplified Schematic




## Features

- $R_{DS(on)}$ = 6.0mΩ( Max.)@ $V_{GS}$ = -10V, $I_D$ = -20A
- $R_{DS(on)}$ = 9.7mΩ( Max.)@ $V_{GS}$ = -4.5V, $I_D$ = -15A
- Extended $V_{GS}$ range (-25V) for battery applications
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- RoHS compliant

## MARKING DIAGRAM & PIN ASSIGNMENT




SO-8

## Absolute Maximum Ratings ($T_A$ = 25℃ unless otherwise noted)

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | -30 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | Drain Current -Continuous | (Note 1a) | -20 | A |
| | -Pulsed | | -69 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 3.8 | W |
| | | (Note 1b) | 1.5 | |
| | | (Note 1c) | 1.2 | |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | | -55 to +150 | °C |

## Thermal Characteristics

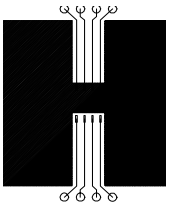
| | | | |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance , Junction to Ambient (Note 1a) | 55 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance , Junction to Case (Note 1) | 28 | °C/W |

## Electrical Characteristics $T_J$ = 25°C unless otherwise noted

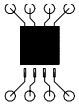
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $B_{VDSS}$ | Drain to Source Breakdown Voltage | $I_D$ = -250μA, $V_{GS}$ = 0V | -30 | | | V |
| $\frac{\Delta B_{VDSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = -250μA, referenced to 25°C | | -20 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -24V, $V_{GS}$=0V | | | -1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±25V, $V_{DS}$=0V | | | ±10 | μA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = -250μA | -1 | -1.5 | -2.5V | |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = -250μA, referenced to 25°C | | 6.5 | | mV/°C |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = -10V, $I_D$ = -13A | | 6 | 10 | mΩ |
| | | $V_{GS}$ = -4.5V, $I_D$ = -11A | | 11 | 14 | |
| | | $V_{GS}$ = -10V, $I_D$ = -13A, $T_J$ = 125°C | | 15 | 18 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = -5V, $I_D$ = -13A | | 34 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -15V, $V_{GS}$ = 0V, f = 1MHz | | 3240 | | pF |
| $C_{oss}$ | Output Capacitance | | | 380 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 231 | | pF |
| **Switching Characteristics (Note 2)** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = -15V, $I_D$ = -1A, $V_{GS}$ = -10V, $R_{GS}$ = 6Ω | | 21 | | ns |
| $t_r$ | Rise Time | | | 18 | | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 26 | | ns |
| $t_f$ | Fall Time | | | 8 | | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = -15V, $V_{GS}$ = -10V, $I_D$ = -13A | | 98 | | nC |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = -15V, $V_{GS}$ = -5V, $I_D$ = -13A | | 61 | | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | 7.5 | | nC |
| $Q_{gd}$ | Gate to Drain Charge | | | 15.5 | | nC |
| **Drain-Source Diode Characteristic** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = -2.1A | | -0.7 | -1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = -13A, di/dt = 100A/μs | | | 40 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | $I_F$ = -13A, di/dt = 100A/μs | | | -31 | nC |

**Notes:**

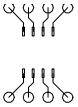
**1:** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 $in^2$ pad of 2 oz copper



b)105°C/W when mounted on a .04 $in^2$ pad of 2 oz copper



c) 125°C/W when mounted on a minimun pad

Scale 1 : 1 on letter size paper

**2:** Pulse Test:Pulse Width <300μs, Duty Cycle <2.0%

**3:** The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

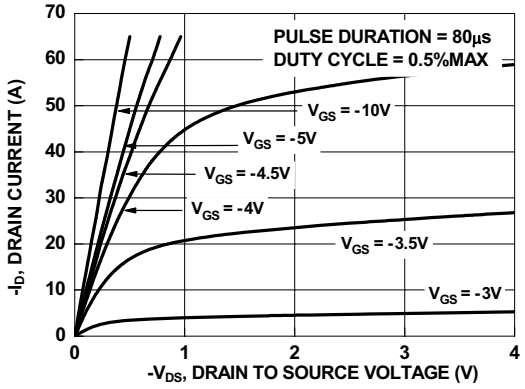



**Figure 1. On Region Characteristics**

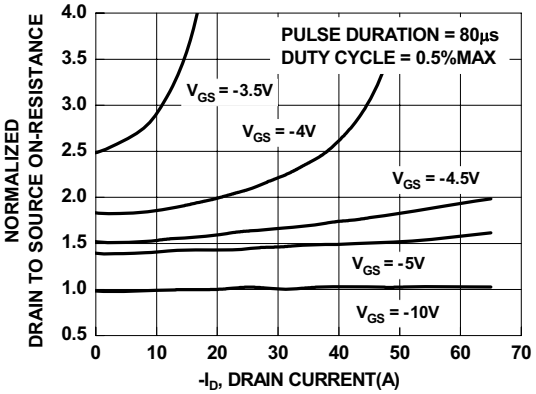



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

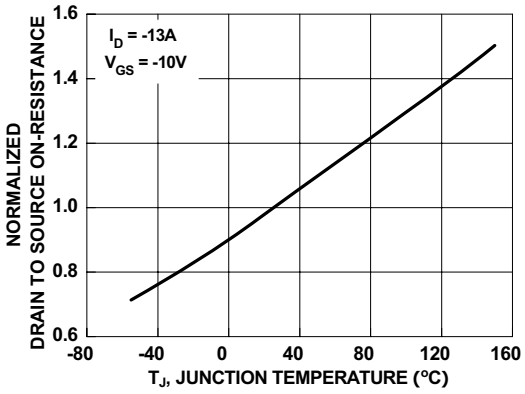



**Figure 3. Normalized On Resistance vs Junction Temperature**

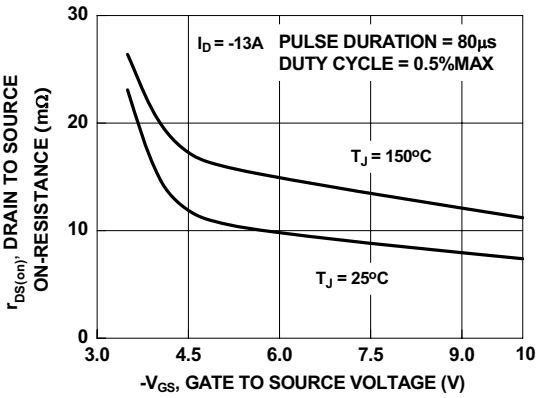



**Figure 4. On-Resistance vs Gate to Source Voltage**

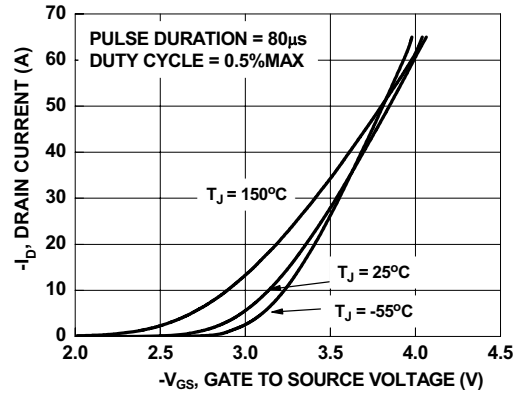



**Figure 5. Transfer Characteristics**

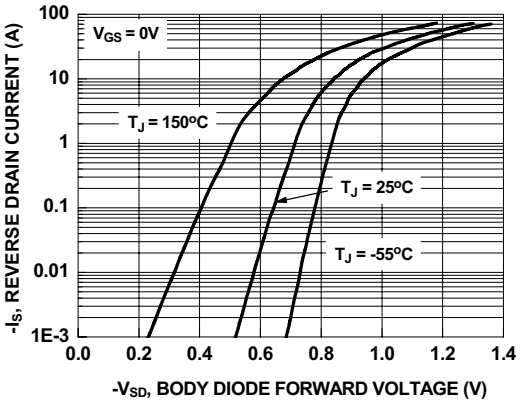



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

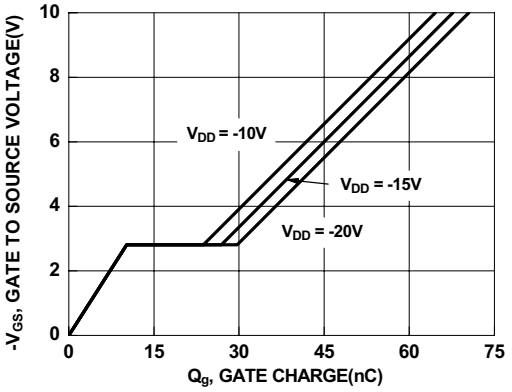



**Figure 7. Gate Charge Characteristics**

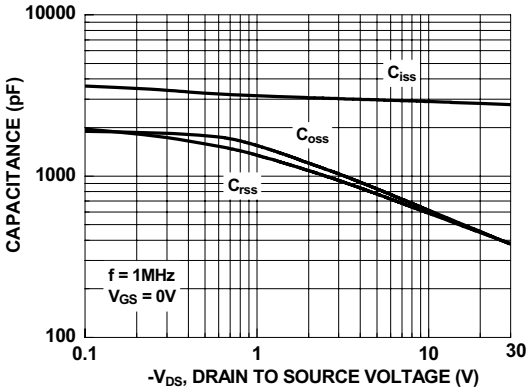



**Figure 8. Capacitance vs Drain to Source Voltage**

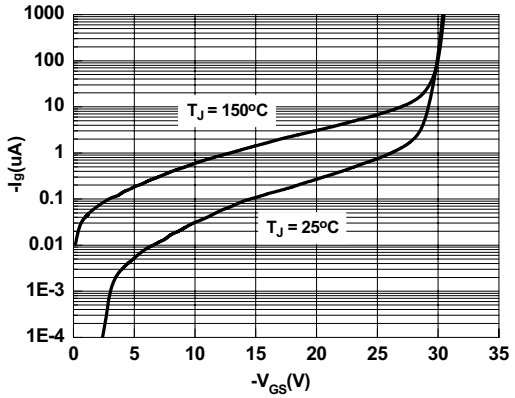



**Figure 9. $I_g$ vs $V_{GS}$**

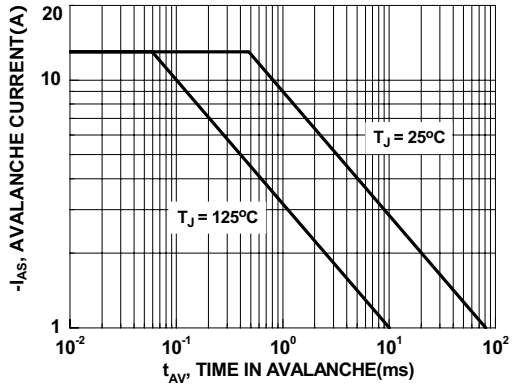



**Figure 10. Unclamped Inductive Switching Capability**

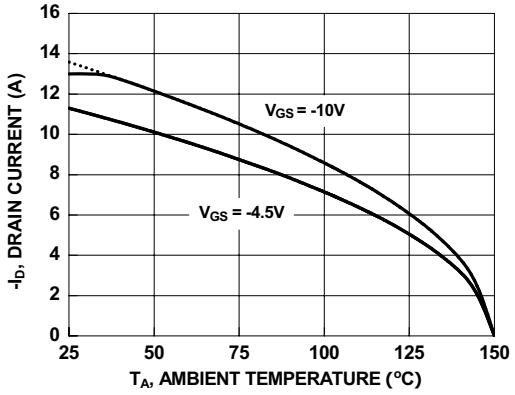



**Figure 11. Maximum Continuous Drain Current vs Ambient Temperature**

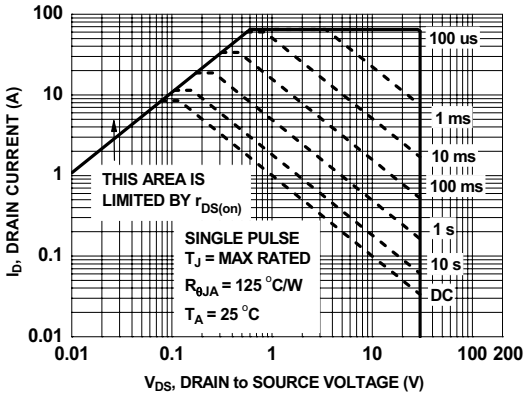



**Figure 12. Forward Bias Safe Operating Area**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

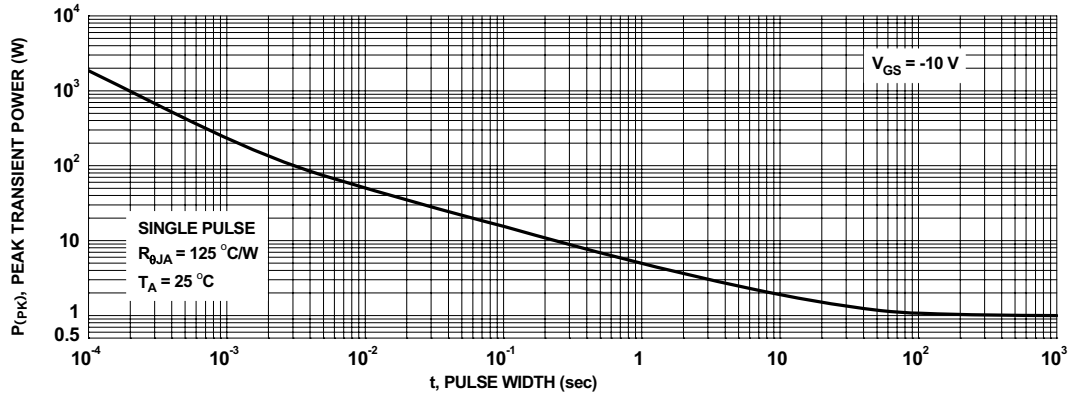



**Figure 13. Single Pulse Maximum Power Dissipation**

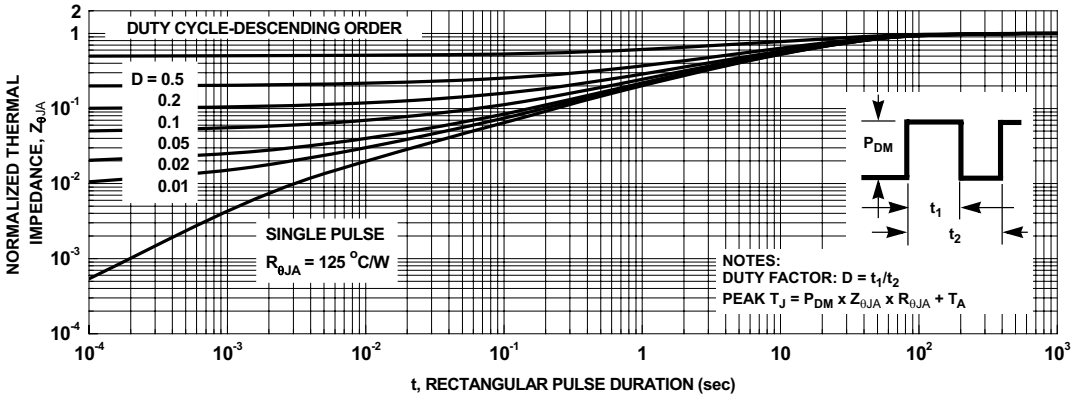
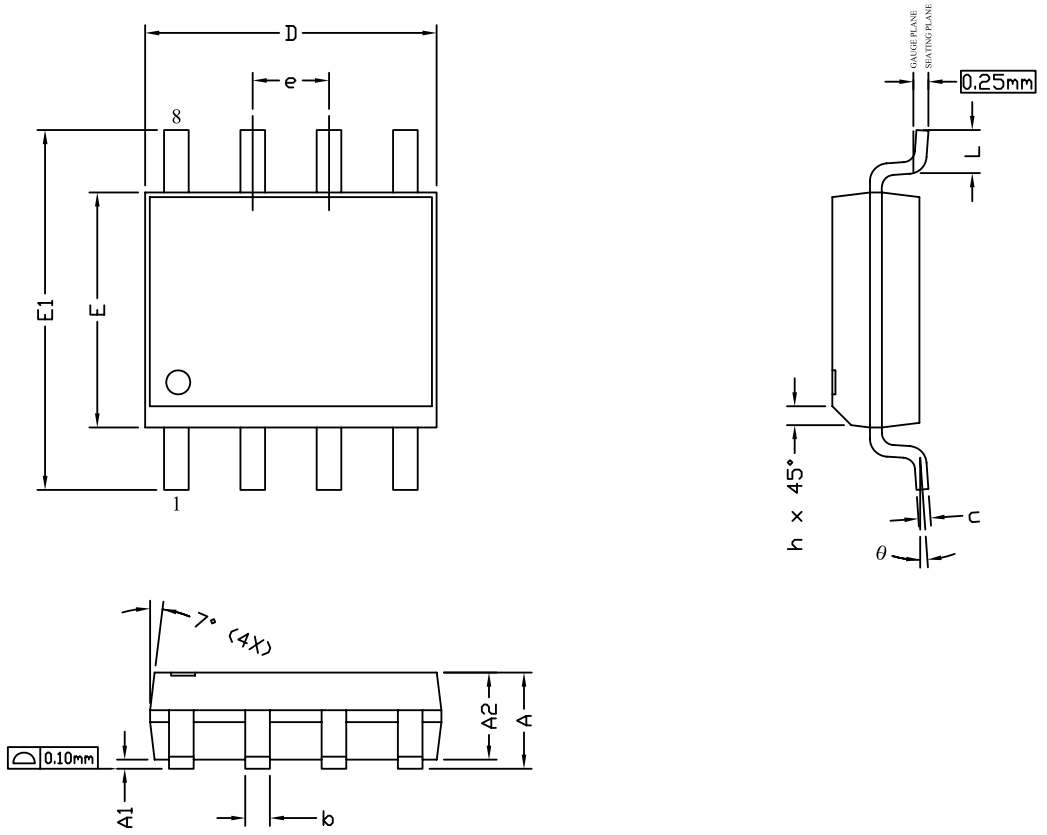


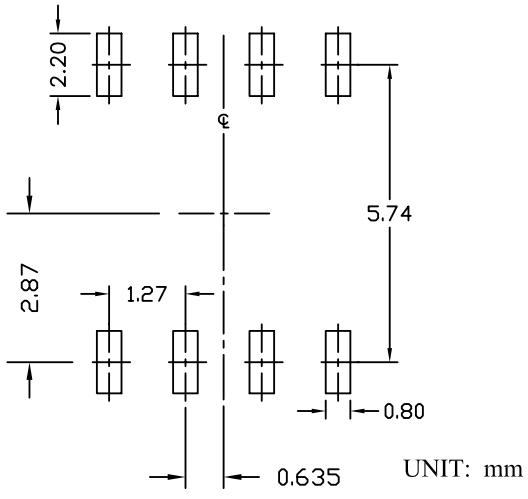

**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**

| Document No. | PO−00004 |
|---|---|
| Version | rev H |

# SO8 PACKAGE OUTLINE




## RECOMMENDED LAND PATTERN




| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.35 | 1.65 | 1.75 | 0.053 | 0.065 | 0.069 |
| A1 | 0.10 | ––– | 0.25 | 0.004 | ––– | 0.010 |
| A2 | 1.25 | 1.50 | 1.65 | 0.049 | 0.059 | 0.065 |
| b | 0.31 | ––– | 0.51 | 0.012 | ––– | 0.020 |
| c | 0.17 | ––– | 0.25 | 0.007 | ––– | 0.010 |
| D | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| E | 3.80 | 3.90 | 4.00 | 0.150 | 0.154 | 0.157 |
| e | 1.27 BSC | | | 0.050 BSC | | |
| E1 | 5.80 | 6.00 | 6.20 | 0.228 | 0.236 | 0.244 |
| h | 0.25 | ––– | 0.50 | 0.010 | ––– | 0.020 |
| L | 0.40 | ––– | 1.27 | 0.016 | ––– | 0.050 |
| θ | 0° | ––– | 8° | 0° | ––– | 8° |

NOTE
1. ALL DIMENSIONS ARE IN MILLMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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### Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.