MT82P50N3

P-Channel Enhancement Mode Field Effect Transistor

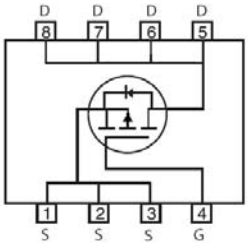
MT Semiconductor®

http://www.mtsemi.com

Product Summary

- V_{DS}= -20V
- I_D = -50A
- $R_{DS(ON)}$ = 5.5mΩ @V_{GS}= -10V
- $R_{DS(ON)}$ = 6.5mΩ @V_{GS}= -4.5V
- $R_{DS(ON)}$ = 8.0mΩ @V_{GS}= -2.5V
- $R_{DS(ON)}$ = 10 mΩ @V_{GS} = -1.8V

Simplified Schematic

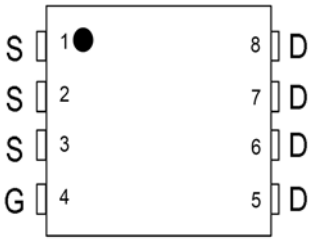


Features

Advanced Trench Process Technology.

- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

MARKING DIAGRAM & PIN ASSIGNMENT



DFN3X3-8L

Applications

- Notebook Computer
- Portable Battery Pack

Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-50	A
Drain Current-Pulsed (Note 1)	I_{DM}	-150	A
Maximum Power Dissipation	P_D	2.6	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	40	℃/W

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT82P50N3	MT82P50N3	DFN3X3-8L	7"	8mm	3000 units

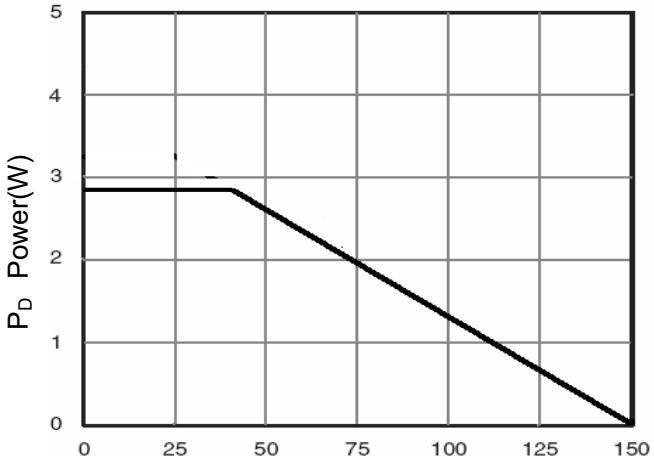
Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-16V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.4	-0.6	-1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-8A	-	6.5	12	mΩ
		V_{GS}=-2.5V, I_D=-6A	-	8.0	16	mΩ
		V_{GS}=-1.8V, I_D=-5A	-	10.0	18	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-15A	30	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz	-	2910	-	PF
Output Capacitance	C_{oss}		-	420	-	PF
Reverse Transfer Capacitance	C_{rss}		-	280	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-15V, ID=-10A, V_{GS}=-10V,R_{GEN}=6Ω	-	16	-	nS
Turn-on Rise Time	t_r		-	12	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	t_f		-	21	-	nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-10A,V_{GS}=-10V	-	48	-	nC
Gate-Source Charge	Q_{gs}		-	12	-	nC
Gate-Drain Charge	Q_{gd}		-	14	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-8A	-	-	-0.7	V

Notes

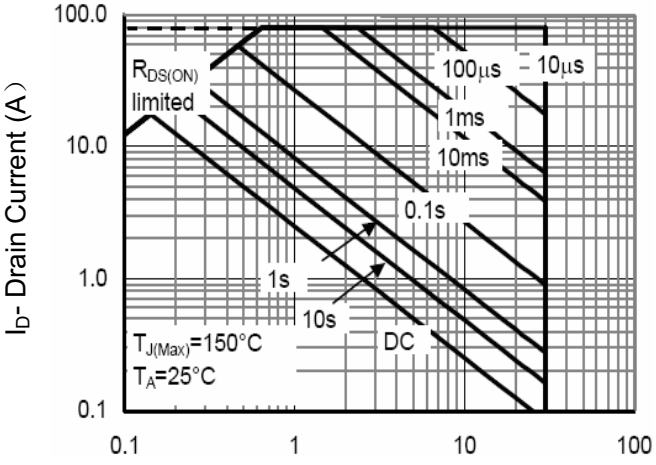
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Characteristics Curve (T_A=25°C, unless otherwise noted)



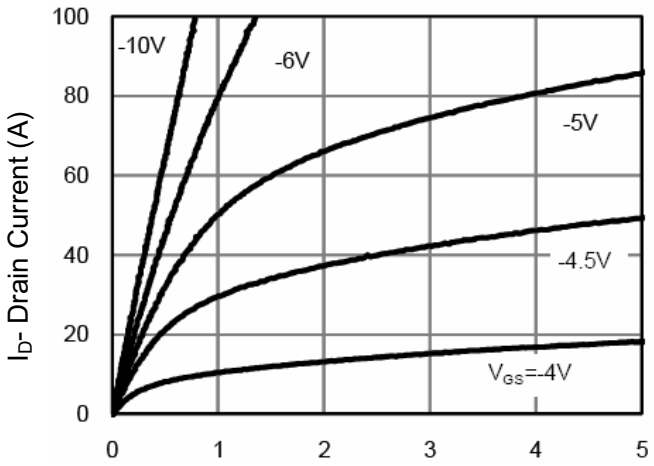
T_J-Junction Temperature(℃)

Figure 1 Power Dissipation



Vds Drain-Source Voltage (V)

Figure 2 Safe Operation Area



Vds Drain-Source Voltage (V)

Figure 3 Output Characteristics

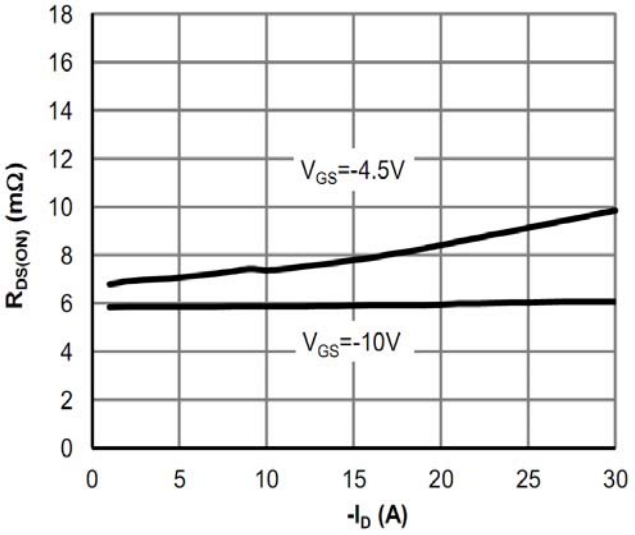
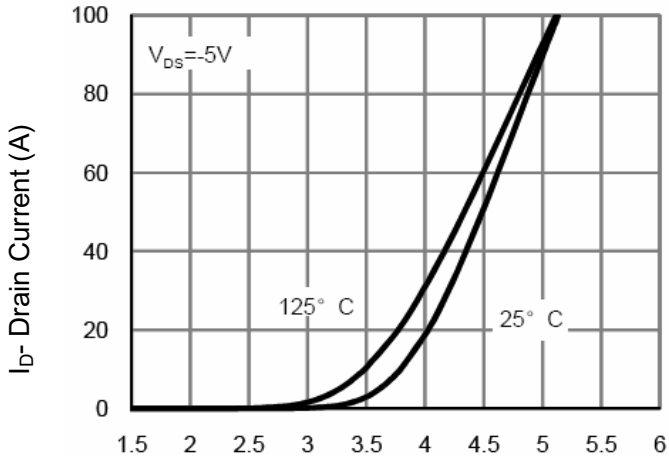
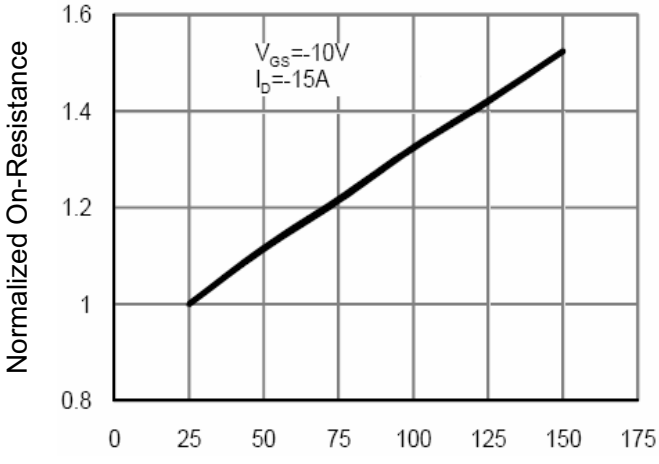


Figure 4 Drain-Source On-Resistance



Vgs Gate-Source Voltage (V)

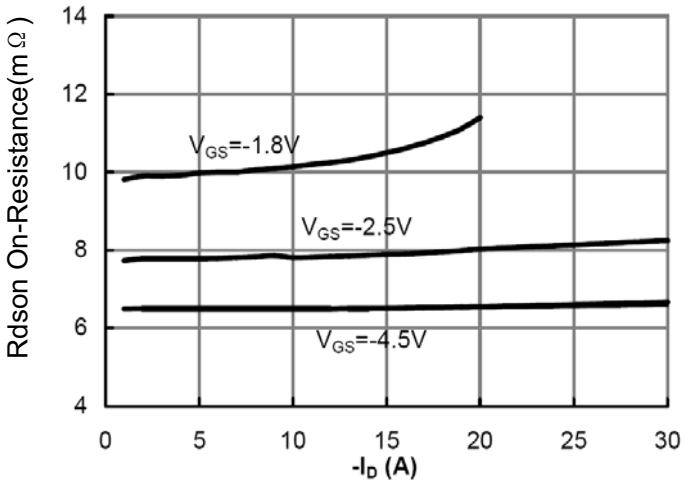
Figure 5 Transfer Characteristics



T_J-Junction Temperature(℃)

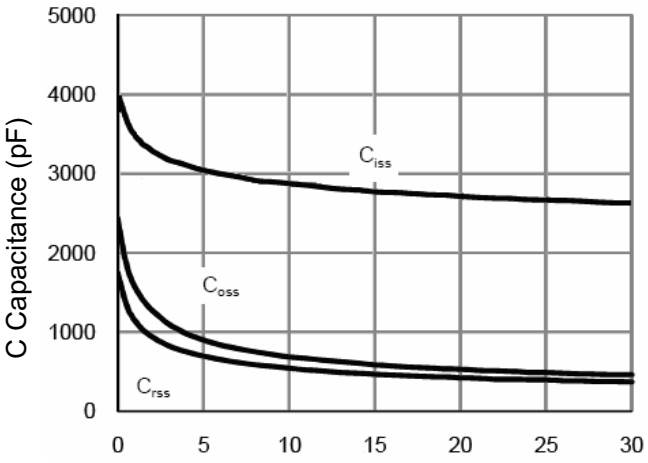
Figure 6 Drain-Source On-Resistance

Characteristics Curve (T_A=25°C, unless otherwise noted)



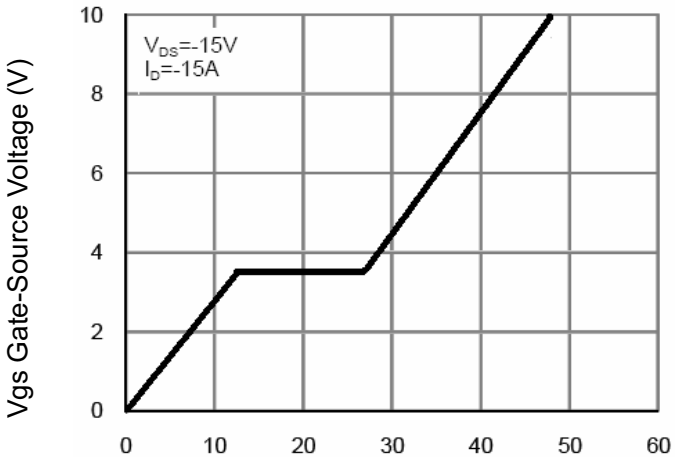
Vgs Gate-Source Voltage (V)

Figure 7 Rdson vs Vgs



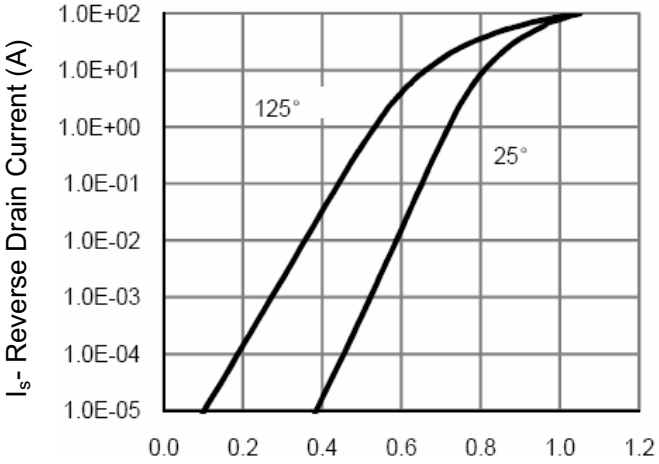
Vds Drain-Source Voltage (V)

Figure 8 Capacitance vs Vds



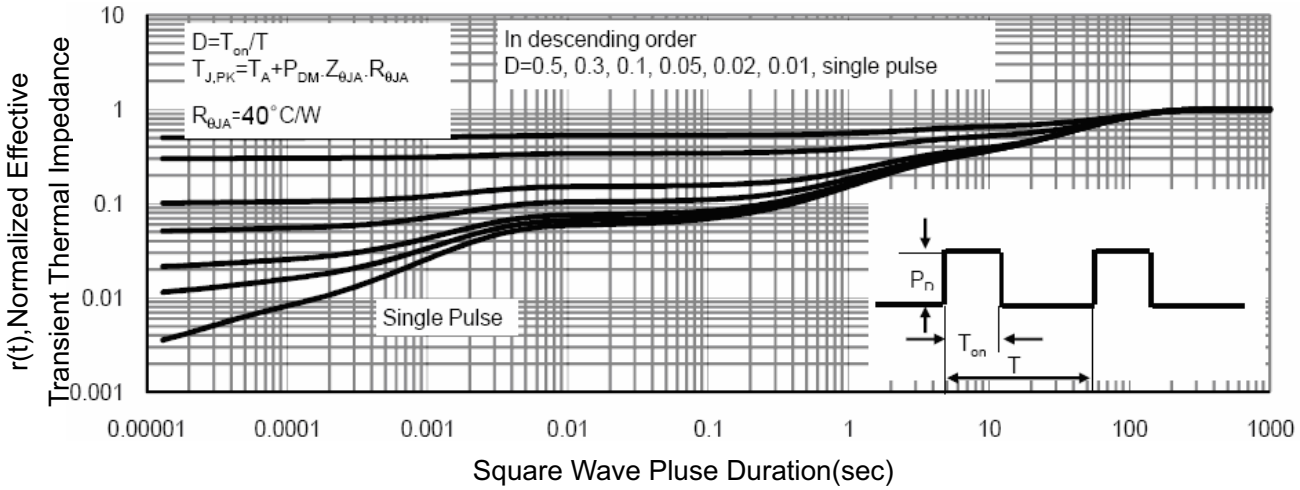
Qg Gate Charge (nC)

Figure 9 Gate Charge



Vsd Source-Drain Voltage (V)

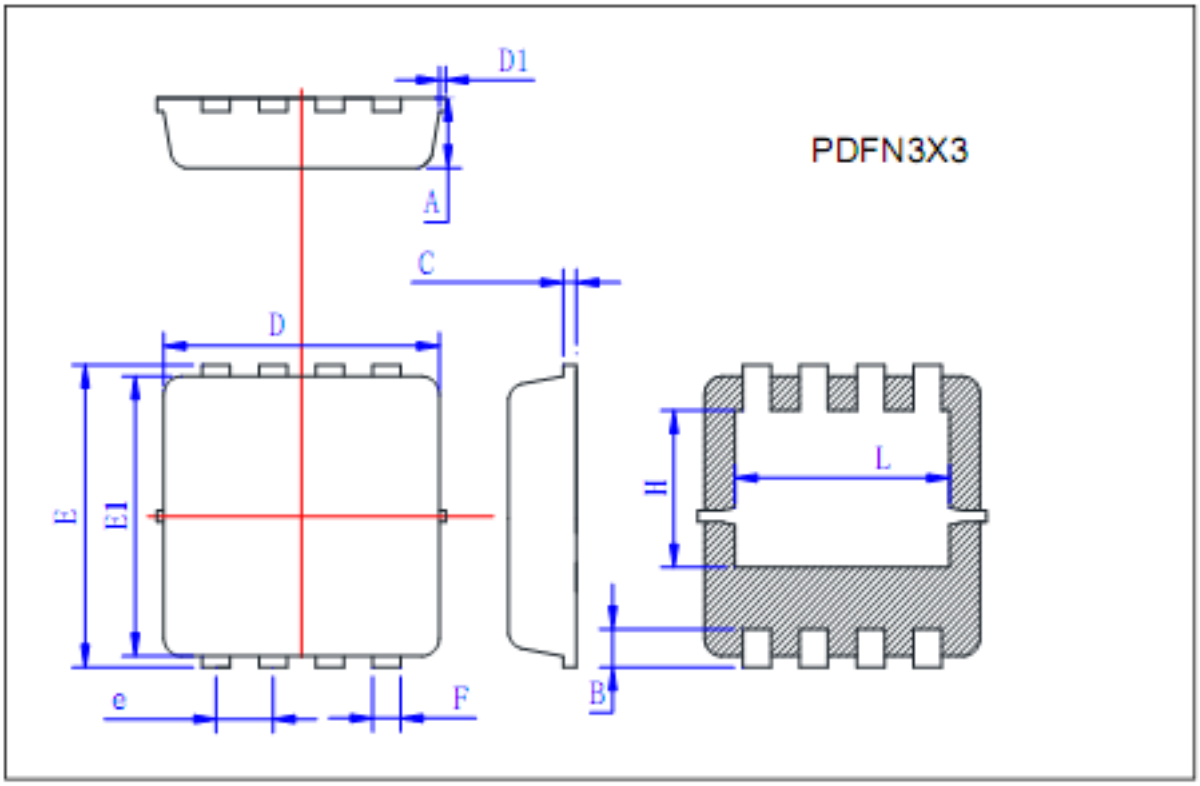
Figure 10 Source- Drain Diode Forward



Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance

PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	2.35	2.45	2.55

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